WHAT IS CLAIMED IS:

1. An emitter coupled logic circuit with a data reload function, comprising:

a differential pair of bipolar junction transistors having a first bipolar junction transistor and a second bipolar junction transistor, each of the bipolar junction transistors having an emitter connected to each other, and a base for receiving a differential signal;

a pair of load resistors consisting of a first load resistor and a second load resistor, each load resistor having a first terminal connected to the collector of the differential pair of bipolar junction transistors, and a second terminal connected to a high operation voltage source;

a resistor connected to the emitters of the differential pair of bipolar junction transistors;

a current source connected to the resistor and a low operation voltage source;

first in series transistors having a third bipolar junction transistor and a first field effect transistor, wherein the third bipolar junction transistor has a collector connected to a collector of the first bipolar junction transistor, a base for receiving a reload signal, and an emitter connected to a drain of the first field effect transistor, while the first field effect transistor has a source connected to the current source, and a gate for receiving the reload data;

an inverter for inverting the reload data; and

second in series transistors having a fourth bipolar junction transistor and a

second field effect transistor, wherein the fourth bipolar junction transistor has a collector connected to a collector of the second bipolar junction transistor, a base for receiving the reload signal, and an emitter connected to a drain of the second field effect transistor, while the second field effect transistor has a source connected to the current source, and a gate for receiving output data from the inverter.

2. The emitter coupled logic circuit according to claim 1, wherein the collector of the fourth bipolar junction transistor is a first output terminal.

3. The emitter coupled logic circuit according to claim 1, wherein the collector of the third bipolar junction transistor is a second output terminal.

4. The emitter coupled logic circuit according to claim 1, wherein the differential pair of bipolar junction transistors can be replaced by an AND architecture.

5. The emitter coupled logic circuit according to claim 1, wherein the differential pair of bipolar junction transistors can be replaced by a latch architecture.